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Exploring the Efficiency and Feasibility of Tin/Al_2O_3/p-Si MIS Devices: A Critical Review and Analysis

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Abstract

Test results have indicated the types of behaviors that can be expected with band engineering. The high-k dielectric used has introduced a mid-gap state in the silicon band gap. It is the Al_2O_3 layer that is causing this. By taking a polycrystalline high-k dielectric, the different grain boundaries that occur in the structure introduce different energies in the insulator layer. The electrons in the silicon that are being pinned are being trapped by these high and low energy states between the oxygen and silicon bonds. This is known as a quasi-static trapping. What this does is build up a positive oxide charge over time. This has an effect on the overall conductance of the p-type silicon. In terms of positive ion charge that is felt by the silicon, the charge density is still the same with electrons being spatially redistributed around the bonding sites. This is a key advantage with high-k dielectrics and one of the goals of the current research into MIS devices. The test data is showing a current increase from the field emission. When tested with constant voltage and varying temperature, the emission is a result of a thermally activated process by the tunneling increases. Energy is transferable to electrons in the silicon with carriers increased and at higher temperatures the increase in carriers is exponential. This can cause negative bias instability in the device and is not a desirable outcome for p-type or CMOS with progression into more advanced technology in the quest for higher device integration. This issue can potentially be resolved by band engineering the silicon. This is a large and complex topic and according to results and the current understanding of high-k dielectrics, no further progress should be made until it is fully understood how an insulator with a mid-gap state can affect the silicon. This and the effects of positive charge build up are the research topics which will lead on from the current work into MIS devices with high-k dielectrics.

Keywords: MIS devise; High-K; Al_2O_3; nanoelectronics; CMOS

Introduction

In microelectronic systems and in any electronic devices, the essential performance of the device is governed by the type of metal-insulator-semiconductor (MIS) interface it uses [1]. This is crucial for the precise control and incorporation of the desired properties into the microelectronic device. This point could not be better exemplified than in the recent progression of high-k dielectrics for metal oxide semiconductor (MOS) gate dielectric. The perpetual scaling down of complementary metal-oxide semiconductors (CMOS) devices has foreground the interest in an ideal dielectric with high permittivity (high-k) as a replacement for SiO_2. The advanced high-k material should exhibit characteristics such as a large band gap, thermodynamic stability in contact with Si, and a reasonable conduction band offset. This is all aimed to increase the control on the gate electrode of this MOS device and, in turn, improve the short channel effects, decrease the gate leakage current, and increase the mobility in the device [2]. One method of creating a MIS device with a high-k dielectric is to deposit the high-k material directly onto a Si substrate using physical vapor deposition (PVD) or atomic layer deposition (ALD) processes [3]. An example of a high-k dielectric is aluminum oxide (Al_2O_3), which has a dielectric constant (k) between 8 and 12 [4]. This opens up a large window of opportunity to improve device performance through the incorporation of Al_2O_3 as compared to SiO_2, which has a k value of therefore the MOS devices of today.

Modern semiconductor devices play a pivotal role in our increasingly digitized world, enabling the functionality of a plethora of electronic gadgets and systems that have become indispensable in our daily lives. Within this realm, Metal-Insulator-Semiconductor (MIS) devices stand out as fundamental building blocks, forming the backbone of various electronic circuits and systems. These devices are pivotal in the realms of digital logic, memory storage, and analog signal processing, among other applications.

Central to the performance and miniaturization of MIS devices is the choice of materials and fabrication techniques. In recent years, the integration of high-k dielectrics has emerged as a critical advancement in semiconductor technology. Dielectric materials with a high relative permittivity (k) offer several advantages over traditional silicon dioxide (SiO_2) dielectrics, including reduced leakage currents, enhanced gate control, and improved scalability.

The significance of high-k dielectrics lies in their ability to address the challenges posed by the continual shrinking of device dimensions in accordance with Moore's Law. As transistor dimensions approach atomic scales, conventional SiO_2 dielectrics encounter fundamental limitations, such as increased leakage currents due to tunneling effects and diminished gate control resulting from direct tunneling phenomena. High-k dielectrics mitigate these challenges by providing higher capacitance per unit area, thereby enabling effective gate control at reduced thicknesses.

Moreover, the integration of high-k dielectrics facilitates the realization of novel device architectures and functionalities. By enabling the fabrication of ultrathin dielectric layers, these materials enable the development of advanced transistor structures such as FinFETs (Fin Field-Effect Transistors) and Gate-All-Around (GAA) transistors, which exhibit superior electrostatic control and reduced short-channel effects compared to conventional planar devices.

In this paper, we delve into the significance of MIS devices in modern semiconductor technology and explore the pivotal role played by high-k dielectrics in enhancing device performance, scalability, and functionality. Through a comprehensive review of the underlying principles, materials considerations, and technological advancements, we aim to provide insights into the current state-of-the-art and future prospects in this rapidly evolving field.

Background

An interesting proposition for the modification of the p-MIS device to rate its potential in the field of high-speed logic circuits is to use an Al/SiC Schottky barrier as its gate. This is attributed to the success of the same modification done to an Al/Y_2O_3/p-Si device, which shows enhancement in device characteristics compared to a standard MOS device. Unfortunately, there is no further re-

search on this Al/SiC p-MIS device, so it is hard to say anything about its potential. Most conventional MOS devices have employed SiO_2 as their insulator because it has a rather high K value compared to other materials. Obtaining the MIS device to work with SiC requires finding an insulator with a suitable low K value. So that is our motivation to do this research on a p-MIS device with an Al/SiC gate at various K values of insulator with Al_2O_3 as the high K material. This is driven by the fact that high voltage or power MIS devices have utilized SiC as the semiconductor or to make more reliable device ionizing radiation-sensitive circuits [5].

Based on these considerations, the study of high voltage MIS devices is interesting and promising. Here we take into the specific example of high voltage MIS devices using p-type silicon as the substrate. Not much research has been done into this type of device, which is odd considering p-type silicon is still the most widely used material of integrated circuits today. An example of a possible application of this device is in voltage mode logic gate circuits. It is believed that such circuits have better noise margins when compared to traditional CMOS logic gates. Also, the device's switching speed can be optimized with the right combination of insulator and gate material. So this could be attractive for high-speed logic circuits or RF circuits. All of these would be of great benefit if a simple and cheap process of fabrication could be found.

Metal-insulator-semiconductor (MIS) devices have a high potential in the field of nanoelectronics. This is due to their relative ease of fabrication and the suitability to be scaled down in size. The latter point is a fundamental issue in the technology of current semiconductor devices, which have already achieved traditional MOSFET's dimensions on a nanometer scale [6]. This is driven by the potential to make a more powerful microprocessor or a more reliable memory storage unit. One way to increase the reliability of a semiconductor device on a nanometer scale is by increasing the supply voltage. Because the switching speed of the device is inversely proportional to the supply voltage, increasing the supply voltage can reduce the device's switching speed to a tolerable level. Unfortunately, traditional MOS devices cannot be scaled up in supply voltage more than 2V due to the insulator's lifetime reliability. MIS devices have no such problem as they can be scaled up to 5V as demonstrated in silicon on insulator (SOI) MOSFET [7].

Purpose

Energy distribution at intermediate temperature range, i.e. from very low temperature to room temperature, is a promising and interesting field of research. Very low and especially roughly room temperature because in this record various metal oxide semiconductor devices work in favor of transistor action with a particular metal gate. Therefore, the study of electrical properties of these devices would be useful in understanding the device behavior. Varactor diode is commonly based upon Metal Insulator Semiconductor (MIS) capacitor having variable capacitance. Electrical conductivity is one of the most important properties of matter. It is important in fields such as engineering, materials science, condensed matter physics, and the life sciences. All electrical, electronic, and information technology devices and systems in use today rely on efficient data transfer and storage. Power losses during these operations are significant and the annual energy usage is in the same order of magnitude as the world's production of electrical energy. Thus, more efficient storage and transfer of data would have significant environmental and financial benefits. These devices mainly work in high-frequency range. Therefore, the analysis of electrical behavior of the devices at high frequency would be useful.

Device Structure

Tin/Al_2O_3/p-Si MIS Device

In this chapter, we will talk about the development of the proposed MOS capacitor structure, which is a Tin/Al_2O_3/p-Si MOS capacitor [8]. For a long time, the MOS capacitor has been used to determine the quality of the dielectric. If there is a possibility to substitute the dielectric, we need to compare the new dielectric with the previous dielectric in the existing MOS device. Since the high-k dielectric only shows its advantages in the MOSFET structure, we are proposing the high-k dielectric in the MOS capacitor. Usually, it is difficult to measure the D_{it} in the MOSFET structure. If we use the MOS capacitor, it is easier to measure the D_{it}. It is be-

cause the MOS capacitor has a simpler structure compared to the MOSFET. In the MOS capacitor, the difference between the voltage applied to the capacitor with the voltage applied to the dielectric can be neglected, $V_{fb} = V_d$. This condition simplifies the measurement of the threshold voltage since the flat band voltage is equal to the voltage applied to the dielectric. From the capacitance--voltage plot, we can extract the value of the dielectric permittivity and the flat band voltage [8]. With a known value of q and ε, we can calculate the D_{it}. By comparing with the Dit data in the MOSFET, this study has proven that the MOS capacitor has the same effectiveness as the MOSFET to measure the D_{it} [9]. For that purpose, we need to develop a new MOS capacitor structure using the high-k dielectric. Step by step, starting from the Al_2O_3/p-Si MOS capacitor that has been developed by JITRI, we will make a modification to the existing MOS capacitor structure. The first step is to substitute the gold electrode with a Tin electrode [19]. The reason is to prevent the oxidation of gold that will contaminate the Al_2O_3 dielectric. Simulation has shown that the energy levels of the Tin and the gold are not too much different. So, with the same work function, the quality of the capacitance and the C-V plot obtained will be similar to the gold electrode MOS capacitor. The next step is to modify the p-type silicon. This modification is intended to get the energy band diagram similar to the p-type Si in the MOSFET. It is necessary because before realizing the MIS device, it is required that the devices developed have the same characteristics as the previous device. By considering the simplicity of the p-type Si in the MOSFET, we are making a trial with the p-type dopant concentration in the order of 10^{17}-10^{18} cm^{-3}. With an energy band diagram similar to the p-type Si in the MOSFET, it is expected that the p-type p-TiO_2 annealed semiconductor can be developed to be used as the channel for the CMOS gate stack structure.

High-K MIS Device

In the present day, the thickness of gate oxide has approached down to 3.5nm to have a bigger field impact on mobility. Because of such little thickness, the solidity of SiO_2 gets influenced antagonistically. For instance, leakage current increments and unwavering quality against voltage debases. To get rid of this issue, the change of door dielectric from SiO_2 to materials that have a more prominent permittivity than SiO_2 has been considered. One of the up-and-comers is Aluminum Oxide (Al_2O_3), which has a dielectric steady that is multiple times greater than SiO_2. To have a more noteworthy decrease in leakage current, TiN, which is a high melting point metal and makes a good Schottky contact with Si and is useful for its alternative as a door material, has been utilized. By inserting a thin layer of high-k material between the gate dielectric and silicon, it is conceivable to enhance the channel. This gadget is known as a MIS (Metal-Insulator-Semiconductor) Device. P-Si channel type was become acquainted with having a more prominent field-impact mobility. To increase better agreement, gadgets were worked for both forward and reverse mode operations. Ideal enhancement mode operation ($Q_n > 0$) was seen in C-V characteristics for the reverse operation ($Q_n < 0$). This operation is used to check the amount of qualitative shift in the channel towards inversion or accumulation. In our case, it is used to check whether a p-type channel has been made. By noting the slope of Q_n vs V plot, it can be deduced that current devices are good for low power consumption as expected [10].

Material Properties

Tin Properties

One of the driving forces in the increase of the high interest in tin is not just the experimentation of the single element itself, but thin films on other insulators and metals to employ the use of the high-k dielectric. Investigations on Tin oxides have recognized that there are many different structures of SnOx and each of these and the method of construction on p-type Si affects the electronic properties [24]. Tin has many different oxides due to the many oxidation states of Sn, the most common of these is SnO and SnO_2, both of which are stable and have practical uses. SnO is primarily a compound where only a few studies have recognized the use of conducting it to create a diode. The main attributes of Tin that have driven the work on the Al_2O_3/Sn/p-Si device are the mutability of the oxidation state and it's somewhat likeness to silicon in its p-type doping. Due to the fact that p-Si is the most common form of silicon used in devices, the studies on the various oxides of tin have taken form on this type of Si by dry O_2 annealing a sample within an enclosed vessel at various temperatures. This process actually oxidizes the silicon as well as the thin film of tin

and can result in the creation of SiO_2 at the interface with the Al_2O_3 [11], which has shown to be unstable at certain conditions and can weaken the overall properties of the high-k device. An example of this is shown that when an as-deposited layer of Al_2O_3 on Si is annealed at 1000°C it will crack due to the formation of SiO_2. Studies have found that the plasticity of the oxidation reaction can manipulate the properties of the tin film and the ability to control the thickness of the film with the changing the anneal duration. An increase in oxygen pressure and temperature of the anneal results in a thicker SnO_2 layer and produces an increase in the resistance of the film thus an increase in the amount of O_2 present may have negative effects on the device as the formation of Al_2O_3 requires a low partial pressure of O_2. High resistance is an undesirable attribute for the tin film as it is required to be used at electrodes in thin film devices and the formation of SnO_2 has a scene to produce a homojunction diode with the silicon substrate, although not preferred for an MIS device, this can prove to be a useful attribute in memory devices. Simulation has provided that a thin layer of SnO with minimal SiO_2 would be the optimum configuration with the Al_2O_3 film at room temperatures.

Aluminum Oxide (Al_2O_3) Properties

This section discusses aluminum oxide and its properties, including band structure, bonding type, unit cell and density, dielectric constant, and band gap. Significant attention has been placed on its dielectric constant because in a MIS device, high dielectric constant materials contribute to increasing the capacitance per unit area. Al_2O_3 has a monoclinic unit cell and is also the most stable of the Al_2O_3 phases [12]. Its density is 4.03 g/cm^3 and the band gap is ~6 eV. Al_2O_3 has been fabricated in various ways such as physical vapor deposition, atomic layer deposition, chemical vapor deposition, and spin-on . The differing fabrication methods have led to varying properties, although some generalizations have been made. High-quality Al_2O_3 has a dielectric constant between 7.8-9.0 and a band gap between 7-9 eV. However, for the purposes of the MIS device, the most significant property of Al_2O_3 was the discovery that with high-temperature annealing (~1000°C), the dielectric constant improved to ~11-13 with a smaller band gap at 5.8-6 eV. This suggested that the use of low-temperature Al_2O_3 for the gate oxide and using high-temperature annealed Al_2O_3 for the insulator has strong potential for future MIS devices.

High-K Material Properties

The improvement of the high-k layer properties is one important issue in MIS devices. It is known that the leakage current is quite sensitive to the type of high-k material used. The higher oxide leakage reduction compared to the SiO_2 on similar physical thickness can be preceded by increased permittivity of the dielectric material. This condition is very useful for the next generation of MOS devices design, in order to increase the gate control on channel to get better on and off current switch. The steady state current-voltage characteristics which observed after the electrical measurement data must be understood that the presence of high-k layer on this MIS device was caused shifted of the accumulation capacitance voltage and the leakage current for each voltage applied. The depletion and accumulation capacitance voltage showed in the capacitance-voltage characteristic is a variable to determine the flat band voltage. During the electrical measurement the high frequency data was used in order to avoid the effect of the diffusion current through the interface between the gate and the dielectric material. High k has an effect on reduction of the oxide field and it is known that the oxide field can be reduced about q/k where q is an electronic charge and k is a dielectric constant [13]. The shifting of the depletion and accumulation capacitance voltage must be followed with the reduction of the leakage current slope between these two voltages. The other important properties which need to understand are the breakdown voltage and reliability. The breakdown voltage of a MIS device and the same physical thickness of the oxide layer highly depend on the dielectric constant material. This condition will cause the high-k material needs a thicker oxide layer to get the same quality in comparison with the SiO_2. If only the thickness of the oxide layer is fixed by using the high-k material it is feared that the breakdown voltage will decrease due to the thinning of the oxide layer. High-k material also reduce the reliability of the dielectric layer, it was occurred with the increasing of charge trapping which is caused by the high-k [14]. This condition will reducing the mobility of trapped charge to the electron hole pairs and it will end with the permanent trapped charge in the gate dielectric and it is feared has a effect on a current state into the gate dielectric.

Fabrication Process

The entire fabrication of the proposed devices was done in the Metallurgical Laboratory at the Center for Material Science and Nanotechnology, a major research laboratory under the Department of Physics, University of Oslo. All processing steps were done inside an enclosed system of ULB (Universal Leakage Box) so that the contamination in terms of metal impurities could be avoided. Right after the collection of high purity n-type Si wafer from the store, it was initially soaked in an organic solvent, acetone, for 10 minutes in an ultrasonic and then later cleaned in a similar manner in ethanol. This cleaning was to remove any particles on the Si wafer. After the cleaning, the Si wafer was blow dried in nitrogen, which leaves the Si wafer with a thin layer of oxide. The oxidation was essential because the thin oxide layer known as "pad oxide" prevents metal spiking and suppresses the roughening of the Si-SiO_2 interface, which usually occurs after annealing in high temperature throughout the entire process of fabricating the device. The pad oxide was observed to be somewhere between 250-300nm. An alternative manner in which this can be achieved is to grow the oxide.

Steps Involved in Fabrication

Oxidation: The device used in the experiment was fabricated in the Class 100 clean room at De Montfort University [15]. The first step would be cleaning the silicon wafer using the RCA procedure. This is to remove any organic and inorganic contamination on the wafer, followed by drying the wafer with nitrogen gas and heating it at a temperature for 10 minutes in order to remove the residue of water. The purpose of this step is to make the wafer hydrophobic and easier to be oxidized. The cleaning process of the wafer should result in a clean surface, as it is important before undergoing the oxidation process. The cleanliness of the wafer can be determined by putting it in a water beaker and observing how many seconds it takes for the water to spread on the wafer surface.

Silicon wafer has an inherent ability to be oxidized in a dry or wet environment. This is due to the nature of the silicon atom, which has 4 valence electrons. Oxidation can be used to grow a thick silicon dioxide (SiO_2) layer, which will act as the insulator of the device. The oxidation process is divided into two processes: dry oxidation and wet oxidation. Dry oxidation process will be used for the growth of a thin SiO_2 layer that can be used as the gate area. The wafer is put inside the quartz furnace tube and oxygen gas is flowed with a temperature of 1 atm and 1000 degrees Celsius for 30 minutes. Then, the pattern will be etched with photo resist and the oxide layer will be removed using an etching process. Wet oxidation process will be used for the growth of a thick SiO_2 layer. The oxidation process involves immersing the wafer into water containing oxygen gas at a temperature of 1000 degrees Celsius for 20 minutes.

Patterning: The patterning process involves using photoresist material that undergoes a property change when exposed to radiation. This method acts as a mask ant to protect the wafer from impurities during the wet etching process. Photo resist powder is turned into a thin layer by spin coating process at 3000 rpm for 30 seconds [16]. Then, the wafer is placed in a constant temperature of 150 degrees Celsius to remove the solvent contained in the photoresist. Next, the photoresist is exposed to radiation to change the pattern and image onto the photoresist from the mask. Then, the wafer is placed into a developer solution to remove the metal oxide. This process is done after the photoresist has been exposed to a certain temperature for a period of time. The last process is the hardening process, which aims to increase the resistance of the patterned photoresist when undergoing the wet etching process.

Challenges and Considerations

The high-K dielectric imposes a tough challenge in terms of optimizing the leakage current mechanism. In the study of leakage current mechanisms and conduction in insulators, a general theory for crystalline solids is an accepted point of reference. High-K insulators consist of many dipoles and charge carriers that are situated at or near the conduction band edge. The dipoles become the emission sites and the charge carriers control the conduction mechanism. As conduction and leakage current mechanisms are

mainly dependent on the energy distribution in the insulator and the nature of the insulator band structure, it would be appropriate to use the theory of conduction and leakage current for an insulator with a high K value. Unfortunately, this involves solving complex multidimensional integrals and differential equations for the energy distribution in the insulator, and the solutions are usually in forms of diagrams which are difficult to interpret. Due to the complexity of this theory and the work involved in obtaining the solutions, very few scientists have attempted to apply this theory to high K insulators. One aspect of bonding the Al_2O_3 film that is important to consider is the annealing of the Al_2O_3 film after it has been deposited. The Al_2O_3 insulating layer is to some extent soluble in water, and this can result in problems as the Al_2O_3 can react with the atmosphere and form hydrated oxides. As the bonding in this case involves a water-based wax, this creates the possibility that the Al_2O_3 film will react with the water and wax during bonding [17]. High-temperature annealing increases the rate of reaction and hydrate formation. This can act as a source of charge and cause leakage paths in the insulator. Any solution to this problem would involve an insulator that has no reaction with water and a bonding process that can be performed without heating.

Performance Analysis

Electrical Characteristics

IV measurement for the MIS device Tin/Al_2O_3/p-Si with high-K MIS device shows the electrical behavior of the device when bias is applied. It helps to identify the region where the device operates as the capacitor and region where it behaves like a resistor. Based on the IV measurement, capacitance and conductance mechanism can be identified by using ∂I/∂V analysis. Capacitance voltage measurement helps to determine the changes of semiconductor and dielectric layer properties by showing the graph of C as a function of V applied.

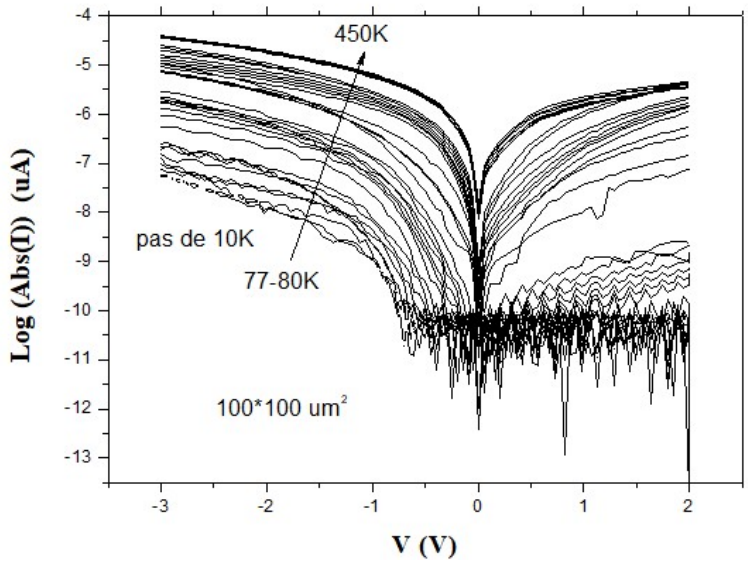

Figure 1: I–V curves of the TiN/Al_2O_3/p-Si structure analyzed at different temperatures.

Figure 1 shows the *I-V-T* curve for the MIS device. Since the curve shows a little leakage current and a high increase in current at high voltage, it can be said that the MIS device is operating in accumulation and threshold voltage, V_{th} region since the slope where ∂I/∂V is high means a high capacitance.

Capacitance-Voltage (C-V) Characteristics

The series capacitors model consists of the oxide capacitance Cox, the interfacial layer capacitance C_{il}, and the semiconductor capacitance Cs formed due to the non-depleted p-Si surface. This shows that the high-frequency capacitance measurements may be able to reveal more information about the behavior of the surface which is not apparent from the conductance measurements. The

simple MIM capacitor consists of two parallel plate capacitors formed by the metal/oxide and the oxide/semiconductor interfaces. An attempt to measure the capacitance of the MIS device was made using an HP4284A Precision LCR Meter at 1 MHz and room temperature. This would give the magnitude of the real part of the capacitance which could not be directly obtained from the conductance measurements, and since the HP4284A has a voltage sweep function, it could provide the C-V characteristics of the MIS device.

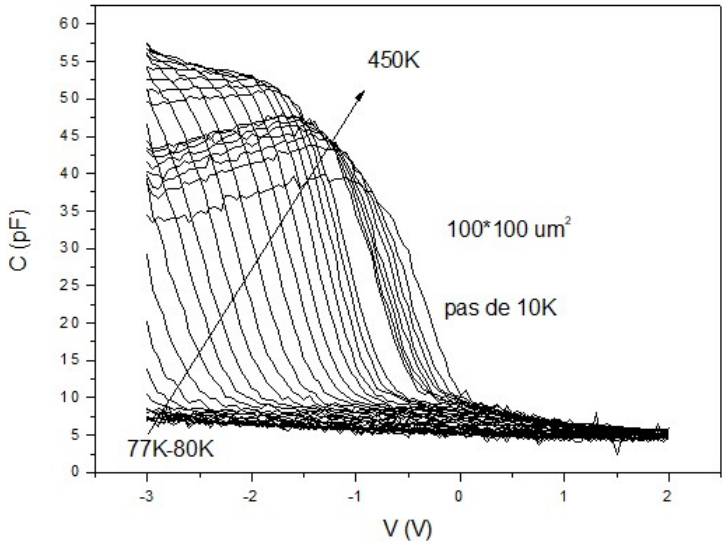

Figure 2: Forward and reverse bias C-V-T characteristics of the TiN/ Al_2O_3 /p-Si Schottky diodes.

During the C-V sweep, the current was monitored by using the voltmeter in the voltage source and it was found that the MIS device was a good insulator as the current flow was in the region of pA which is within the limitations of the meter. A more detailed analysis of the C-V characteristics could be performed at varying frequencies and temperatures. High-frequency C measurements could be attempted using an impedance analyzer with the same V sweep function. An HP4192A LF Impedance Analyzer is available at certain temperatures and this could provide C-V characteristics over a wide frequency and temperature range. Low-frequency capacitance measurements could be conducted at temperatures down to 110K using a Hewlett Packard 16047A test fixture with the HP4284A LCR Meter.

Leakage Current

Leakage currents degrade the performance of the MOS devices. Analysis of leakage current characteristic curves at different temperatures was carried out in order to find the responsible leakage mechanisms prevailing in the present Al_2O_3 (10nm)/p-Si MOS capacitor. To obtain the leakage current characteristics at different temperatures, the current density was measured at an applied voltage of -1MV to 1MV. In general, leakage current is mainly due to the flow of electrons and holes from the valence band and conduction band states of the insulator and the semiconductor.

At lower fields, leakage current is mainly dominated by the Frenkel Pool emission process. When the electric field is high enough, charge carriers gain sufficient energy to overcome the potential barrier of the trapped charge. The good exponential leakage current characteristics on a log scale are a clear indication of Poole-Frenkel conduction occurring near the conduction band. "c" is a constant, "Γ" is the degrees of freedom for transport of carriers in the oxide layer, respectively, "E" the electric field.

The straight line with a slope of 2.3 on the Fowler-Nordheim coordinates for $\Delta V > V_{FB}$ indicates the electron tunneling from p-Si to the Al_2O_3. Substituting the values of the constants, a barrier height of 2.67eV and an oxide thickness of 10nm were obtained. This barrier height is almost coincident with the value of the p-Si surface state density obtained from the C-V measurements. At the higher temperature of 373K, the leakage current characteristics show a different behavior from the electron tunneling process.

It should be noted that there is a small hump on the curve which gradually moves to lower electric fields with increasing temperature. This hump and the non-linear I-V curve associated with it are typical signs of the hopping conduction process. However, the detailed analysis of the data did not enable the distinguishing between the Schottky and Phonon emission processes. In order to clarify which process is valid, a plot of the Fowler-Nordheim coordinates is effective for determining whether the tunneling or the emission rate is dominant.

Comparison with Traditional MIS Devices

Then this section is devoted to discussing the performance of our high-k MIS structure in comparison with traditional MIS devices. It can be clearly seen that the requirement in terms of mobility and/or fixed charge density will be greatly reduced if high-k insulators are used. This follows from the fact that the equation for the flat band voltage for the MIS structure, with a low frequency, high-frequency range and dielectric constant in terms of the applied voltage is given by:

$V_{FB} = (qN(rh - rSiO_2))/(2\varepsilon_0)$

Where V_{FB} is the flat band voltage, ε_0 is the permittivity of free space, r is the insulator dielectric constant, N is the dopant concentration, and q is the charge on an electron. Subscripted terms will refer to the high-k insulator (h) and SiO_2.

With a view to improve the performance of our devices, we consider a low frequency to be greater than the maximum audible frequency, around 20 kHz. This is under the assumption that signal processing at these frequencies will be developed. For devices using Al_2O_3 and a Si = 5 x 10^{17} cm^{-3}, the flat band voltages are V_{FB} = 10.3V for the Al_2O_3 device and 9.1V for the SiO_2 device. This represents a 15% reduction for the device using Al_2O_3.

Semiconductor devices are not only evaluated based on flat band voltage reduction but also on various other critical performance metrics, including device speed, power consumption, and reliability. The integration of high-k dielectrics in Metal-Insulator-Semiconductor (MIS) devices has shown significant improvements in these key areas compared to traditional MIS devices employing silicon dioxide (SiO_2) as the insulating material.

One notable area of improvement is device speed. High-k dielectrics enable faster switching speeds due to their higher dielectric constants. This property enhances the capacitance of the gate insulator, leading to improved charge storage and quicker charge transfer during transistor operation. As a result, MIS devices incorporating high-k dielectrics exhibit enhanced switching speeds, enabling faster operation and improved overall performance in digital logic circuits, memory storage elements, and high-speed communication systems.

Moreover, the adoption of high-k dielectrics contributes to reduced power consumption in semiconductor devices. The increased capacitance per unit area provided by high-k materials allows for effective gate control at thinner insulator thicknesses. Consequently, MIS devices with high-k dielectrics require lower gate voltages to achieve the same level of charge accumulation, leading to reduced power consumption during device operation. This reduction in power consumption is particularly significant in battery-powered electronic devices and energy-efficient computing applications, where minimizing energy consumption is paramount.

Furthermore, high-k dielectrics contribute to enhanced device reliability compared to traditional SiO_2-based MIS devices. The use of high-k materials helps mitigate reliability issues associated with gate leakage currents and dielectric breakdown. High-k dielectrics exhibit lower leakage currents and improved breakdown strength, thereby enhancing the long-term reliability and operational stability of MIS devices. This improved reliability is crucial for semiconductor devices deployed in mission-critical applications, where uninterrupted operation and extended device lifespan are essential requirements.

In summary, the integration of high-k dielectrics in MIS devices offers a host of benefits beyond flat band voltage reduction. These include improved device speed, reduced power consumption, and enhanced reliability, making high-k dielectrics a compelling choice for advancing semiconductor technology and addressing the evolving demands of modern electronic systems.

Advantages of High-K MIS Device

The above discussion has presented that the high-k need to be successfully incorporated into a device for device performance to improve. Although the investigation was conducted for a thin Al_2O_3 layer using aluminum as gate electrode, it is still worthwhile to briefly discuss the advantages of high-k materials in general, by exemplifying the case for Al_2O_3 in two extreme cases with one where modern SiO_2 is employed and another where SiO_2 insulator is not used. High-K dielectric materials not only have high dielectric constant or permitting more electrical charge to be stored per unit volume but also have low leakage current or allowing less charge carriers to move through the dielectric. This will be extremely crucial in facing the challenges of next generation devices scaling where the thickness of gate dielectric below 1.5 nm (corresponding to the capacitance equivalent thickness of less than three atomic layers of SiO_2 and about 10 atomic layers of Si) and gate dielectric will be no longer SiO_2 in order to maintain reasonable drive current with acceptable level of power consumption given the fact that the reduction of gate dielectric thickness is used to increase the gate control on the channel while maintaining the similar gate voltage due to increase in gate insulator area by the use of high-k materials. Low leakage current is due to higher bandgap energy Eg of high-k materials with respect to SiO_2 and less direct tunneling probability at the same thickness and dielectric constant as can be seen from Tunneling current α exp(-B/hw), where h is Planck constant. For application with thin Al_2O_3 it is possible to achieve satisfactory reliability at high fields and low injected charge, because the activation energy for trap formation in Al_2O_3 is highest among high-k material having E form= 2.7 eV and the electron trapping of 10^{-10} C/cm is about 100 times lower than SiO_2 at the same field stress to be doubled with the achievement of less charge as the threshold for oxide breakdown.

Limitations of High-K MIS Device

There are a number of possible limitations to the high-k device outlined in the above. Mentioned was the measurement of D_{it} in the Al_2O_3 layer, considering its thickness is less than 100Å. To accurately measure the value of D_{it} in a high-k dielectric, the CET method, high frequency capacitance transient spectroscopy, and conductance method require the value of D_{it} to be extracted by shifting charges between the high-k layer and the Si substrate and measuring the constant rate. This requires a moderate-high positive or negative voltage on the dielectric layer. Applying this to an Al_2O_3 layer will encounter electron tunneling between the Si substrate and trapping states in the thin (3.5eV) band gap of the Al_2O_3 layer, which is particularly difficult to monitor. A possible solution to this is using the bridging oxygen vacancies to create a vacancy center to trap the charge. This occurs when the oxygen atoms move from non-lattice sites to silicon and/or metal sites, and it has been shown that this can occur if an appropriate voltage and annealing process is applied. Simulation programs and theoretical models have indicated that these E' centers should have a much higher Dit level. This would be an ideal platform to again compare the same device and then insert a SiO_2 layer and compare the two values of D_{it} and the effects on the p-type Si substrate.

Potential Solutions

While high-k dielectrics offer significant advantages over traditional silicon dioxide (SiO_2) in Metal-Insulator-Semiconductor (MIS) devices, they are not without their challenges. One prominent limitation is electron tunneling in thin layers of high-k materials like aluminum oxide (Al_2O_3), which can adversely affect device performance and reliability. However, several potential solutions and mitigation strategies have been proposed to address this issue and provide a more balanced view of high-k MIS devices.

1. Material Engineering:

- Tailoring the composition and structure of high-k dielectrics: By carefully selecting dopants and adjusting deposition parameters, researchers can modify the properties of high-k materials to reduce electron tunneling while maintaining

desirable characteristics such as high permittivity.

- Incorporation of barrier layers: Introducing thin barrier layers between the high-k dielectric and the semiconductor substrate can help mitigate electron tunneling. These barrier layers act as a barrier to electron transport, effectively reducing tunneling currents without compromising other device properties.

2. Thickness Optimization:

- Optimization of dielectric thickness: Controlling the thickness of the high-k dielectric layer is crucial for balancing gate control and tunneling suppression. Optimizing the thickness can help minimize tunneling currents while maintaining adequate gate control for device operation.

- Utilization of thicker dielectric layers: In some cases, using thicker high-k dielectric layers may be preferable to reduce tunneling effects. However, this approach must be balanced with other considerations such as gate capacitance and device performance.

3. Process Optimization:

Improved deposition techniques: Refining deposition techniques such as atomic layer deposition (ALD) and physical vapor deposition (PVD) can enhance the uniformity and quality of high-k dielectric layers, reducing defects and improving tunneling suppression.

Post-processing treatments: Employing post-deposition treatments such as annealing or plasma treatment can modify the properties of high-k dielectrics, potentially reducing tunneling currents and enhancing device performance.

4. Advanced Device Architectures:

- Implementation of novel transistor structures: Exploring alternative transistor architectures such as nanowire transistors or heterostructure devices can offer inherent advantages in tunneling suppression and gate control, mitigating the challenges associated with high-k dielectrics.

- Integration of advanced materials: Combining high-k dielectrics with other advanced materials such as two-dimensional materials or engineered interfaces can provide synergistic effects, enhancing device performance and reliability while minimizing tunneling effects.

By leveraging these solutions and mitigation strategies, researchers and engineers can address the limitations associated with electron tunneling in high-k MIS devices, paving the way for the continued advancement and integration of high-k dielectrics in semiconductor technology. These approaches contribute to a more balanced view of high-k MIS devices, considering both their advantages and challenges in realizing next-generation electronic devices.

Applications

The MIS device is the core component of all kinds of electronic devices, including sensors and new nonvolatile memories. Up to now, silicon-based MIS structures have been studied well and used for a lot of practical devices. Our high-k gate dielectric MIS device can be the alternative of these devices. Figure 33 shows the energy band diagram between the Si and the charge storage layer of our device. In the case of programming VGC positively or negatively, this diagram corresponds to accumulate the holes or electrons to the surface of Si. Both electrons and holes are carriers in usual Si microelectronic devices, and it is preferable to control their transport over a wide region of Si beneath the gate dielectric in order to realize low-kV operation of MIS device. By choosing

the material to be Al_2O_3 with its appropriate energy gap, it can offer wider control margin compared with the case of SiO_2, but we must be careful in order to avoid the avalanche breakdown of Al_2O_3. This wide control margin of carrier transport is advantageous for the application to the low-kV operation devices. The most promising application of ours is the p-channel nonvolatile memory device using the hole as information [18]. In these recent years, the research and development on the nonvolatile memories, such as EEPROM/VL, FRAM and Flash EEPROM, have been carried out actively. From the viewpoint of the simplification and downsizing of information devices in ubiquitous IT society, the higher density and the non-volatileness are the most important features of the memory devices. Flash EEPROM is the most widely used memory device and the high density type realizes the multi-level/-nand-gate cell offers 1 to 2 bit/cell information storage. Since the threshold voltage of the memory cell transistors decides the information and it is regarded to apply the multi level information storage to utilize the controlled carrier transport, it requires over a wide region of Si beneath the gate dielectric and modernization of MIS devices. Our device has all the features required for these applications.

Integrated Circuits

Microelectronics deals with the mass production of electronic components and integrated circuits are the backbone of any electronics system that is being used. It has been predicted that there are high prospects for the use of MIS devices in CMOS technology and the success of CMOS technology by replacing the conventional gate oxides with high-K dielectric layers will be another driving force for MIS technology. This is because the high capacitance of high-K dielectrics provides a thicker equivalent oxide thickness (EOT), thus resulting in reduced direct tunneling current through the gate oxide. With the continuous downscaling of CMOS devices, direct tunneling leakage currents have become a severe issue. This approach will also provide better electrical endurance, enhanced device reliability, and increased junction immunity. Thus, it can be seen that for MIS devices, there will be a transition from metal oxide semiconductor (MOS) devices to metal high-K insulator semiconductor (MHIS) devices [19]. With this in mind, we have taken the first step in using an MHIS device, namely the ALD HfO_2/TiO_2 high-K gate dielectric MOS capacitor, to systematically study the effects of electron and gamma irradiation on the device response and the mechanism and degradation of the gate dielectric. This is because, besides the use of MIS devices for high K CMOS technology, MIS devices have much potential and many uses in radiation environments for space and military applications. With the vast amount of research done on the HfO_2/TiO_2 high-K system in comparison to other high-K systems, this would serve as a sound case study and a benchmark for analyzing the possibilities and limitations of MIS devices for such applications.

Memory Devices

Memory devices have been a long-running interest in electronics as a whole, and with the passage of time, they have evolved from the very simple diode to a multi-storage dynamic RAM. Memory devices can be found on any type of microelectronic system, from the simplest calculator computers to the more complex ones [20]. Both volatile and non-volatile memory devices are used. The former store data as long as power is maintained on to the system and the latter stores data permanently. Examples of this are the floppy disk and the hard disk drives.

A memory storage unit basically consists of a set of integrated circuits which are fabricated on some substrate. The processing of these memory devices may involve high/low temperature steps and different kinds of ion implantation, which means different MIS systems, may be employed. Memory devices store information in the form of bits, and the simplest form is a storage of 1 and 0 that represents binary data. The data is stored in certain locations and must be retrieved in the future, so there must be some form of address to each location. A memory device has a storage capacity and access time. The latter is usually measured in nanoseconds and it is the time required to access stored data after the initial data address.

High charge storage memory devices have been widely researched lately due to their potential in producing very small memory cells. MIS memory devices with a single layer have been studied for a while, and now high-k stack memory devices are becoming more favorable due to the scaling limits of a single layer. High-k devices have the advantage of protecting the underlying silicon

from oxide degradation with a high charge trap density and allowing the use of a thicker high-quality gate dielectric.

Drain and source regions were ion-implanted after MIS capacitor fabrication, and the memory system is an n-channel device. This device shows a large memory window after a post-fabrication annealing and good charge retention up to 10 years at room temperature, where a charge loss of less than 10% is acceptable for the device used in a few years' time. An extended study of this device was done recently by Park et al [21] and Choi et al [22] involving charge retention by monitoring time and conduction and breakdown of the Al_2O_3 layer.

Another form of memory device is the flash memory card, which is a form of EEPROM that can be used to store small data from an experiment in a biology lab to a high-quality image from a digital camera. Recently, a new type of EEPROM memory transistor has been used, known as the metal nanocrystal EEPROM. MIS memory devices of this type have been studied on both a single-layer and a high-k stack device. This device comprises a metal control gate above a Si_3N_4 tunnel dielectric and a semi-spherical nanocrystal layer, which also acts as charge storage sink, on an oxide layer above the n-type silicon substrate. It has been found that a single-layer device has better charge retention due to reduced tunneling out of the charge to the traps in the oxide, but a high-k stack memory device will have a more durable conduction characteristic because it protects the high-quality gate dielectric. An Al_2O_3 layer has been used as the top high-k dielectric layer to protect the nanocrystals from trap charge loss and to increase the endurance window of the device. This is a recent experiment done on a Ta_2O_5 layer [23], and hopefully, more will be done to improve the conduction characteristic of the high-k stack device so that it can be an alternative to the single-layer device.

High-quality memory device research can combine many aspects of MIS device research [24]. In the coming years, there may be a high demand for these devices, and the future technology would possibly be an all-silicon device with some form of a non-silicone gate electrode for a better charge storage capacity.

Sensors

The last part of this analysis of MIS device with high-K dielectric is an investigation on the possibility of this device to be used as a sensor. With the use of ion sensing, the device is tested to explore the interface of the dielectric in low pH solutions. The application of HCl and NaOH with the concentration of 1M to 10^{-6} M has been used to determine the pH sensitivity level of the sensor. Capacitance-Voltage measurements were taken to get the hysteresis graph. This is to measure how much different the flat band voltage is before and after the ion sensing. High hysteresis level of the FBV will decrease device sensitivity. From the C-V measurements, the dielectric leakage current can also be determined. Leakage current will damage the dielectric and also decrease the sensitivity of the device. Results from this ion sensing experiments can give important details on how this device is going to be used as a pH sensor [25].

Other than ion sensing, this MIS device also has the potential to be used as a biosensor. Biological applications that can be tested include DNA detection. Since DNA has a negative charge and large molecule size, it can be suitably detected by measuring the change in the FBV of the device. With the DNA sample in de-ionized water, a +1.5V bias on the Al metal will act as a DNA detection sensor. This is because DNA has a large negative charge and is attracted to the positively charged Al metal. An alternative method is with the use of electrical measurement. An MIS device has the potential to measure the electrical impedance of a biological sample and with the variation of frequency; it can provide accurate details of the tested sample. But of course, before these biological experiments are done, it is necessary to have a thorough analysis on the alkyl and oxide interface to prevent the destruction of the dielectric.

Comparison with Other Devices

MIS devices based on different high dielectrics attached to p-type silicon have been investigated by many researchers for development of low power, high-β and nonvolatile memory devices. A comparison between the various MIS devices has been summarized in many researches. It is clear that the memory window of our device is quite high with very low operating voltage as compared to other high-κ MIS devices fabricated on silicon substrates. The memory window of our device is almost 3 times higher than β-Ta_2O_5 MIS device with same operating voltage. In DRAMs memory window is defined as the potential difference between the voltage at which charge is stored in the dielectric and the voltage at which charge leaks away from the cell. A very high memory window is generally desired for low power SRAM and DRAM applications as it determines the minimum supply voltage and retention time respectively. Although the β value in our case is less than β-Ta_2O_5 MIS device, it is still higher compared to the devices with other high dielectrics. The lower β value can be associated with the high κ value of the dielectric, since β is directly proportional to the κ of the dielectric. But as it has been mentioned earlier the β value of a device should be chosen optimally depending on the memory window and operating voltage of the device [26]. Our MIS device can be effectively utilized for low power SRAM (min $\beta=100\mu A/V^2$) and e-DRAM ($10\mu A/V^2 < \beta < 100\mu A/V^2$) applications.

Tin/Al_2O_3/p-Si MIS Device vs. Other MIS Devices

The Tin/Al_2O_3/p-Si device has recently emerged as the best capacitor, bearing in mind the high-k field. The high-k value for Tin (k = 88) and Al_2O_3 (k = 9 - 11) against the conventional SiO_2 (k = 3.9) has generated much interest. As stated earlier, the high-k materials suffer contamination problem with Si and even Al_2O_3 form silicate layer on Si interface. The Frenkel-Pool-Rossleau model describing the thermodynamic roughening transition is only confined to materials of similar structures. This suggests that the application of Al_2O_3 on SiC or Si_3N_4 on Si are more stable structures, but therein lies the transition problem whereby Si_3N_4 on Si is thermodynamically going to form Si_3N_4 on Si_3N_4 structure. Binding this with the fact that structural stability is subjected to the assertion that the upper layer should possess higher surface energy than the lower layer and the applied field should be kept at a minimum. This inadvertently restricts the field of application of high-k material devices. Despite this, Al_2O_3 has been reported to produce good C-V characteristics and breakdown field of 8MV/cm. However, the compatibility with Si devices is an important issue and the conventional Si - SiO2 structure is still relevant in today's rapid progress of semiconductor technology. Only SiO_2 has better C-V characteristics and breakdown field than Al_2O_3, but the present emphasis is put on the high-k materials. The material compatibility issue is cleared with avoiding Si and Al_2O_3 contact and using thermal Al_2O_3 growth to form double layer Al_2O_3 - SiO_2 films. From this revealed SnO_2 on Si devices still maintain a superior electrical behavior with Al_2O_3 films and Si_3N_4 because of the dielectrically lower SnO_2 and the possibility of an oxygen removing anneal to obtain SnO_2 – Tin - Al_2O_3 structures. It was stated that Si3N4 and O-Ta films on n-type SiC produced excellent C-V characteristics with Al_2O_3 field, but SiC structures limits the scope of application. This furthers the idea that the best MIS devices with high-k materials are not necessarily with the high-k material on high-k material structures.

High-K MIS Device vs. Other High-K Devices

The authors in this paper used the structure Tin/Al_2O_3/p-Si to compare the high-K material they used with other high-K materials that are already in the research. We just compared the electrical characteristics, which are the capacitance voltage characteristics (CV), the leakage current, and the dielectric constant (K) of all high-K materials. In order to compare the characteristics, we needed to know about the other materials used as comparison materials. The other materials they used as comparison materials are HfO_2 and ZrO_2, both of which are high-K materials. HfO_2 is a good candidate for replacing SiO_2 as a gate dielectric material in metal-oxide-semiconductor (MOS) devices due to its high dielectric constant, large band gap, and compatibility with silicon technology. It has attracted much attention for dynamic random access memory (DRAM) capacitors and metal oxide field effect transistors (MOSFETs) because of the scaling of the equivalent oxide thickness of SiO_2 to the physical nitrided thickness of SiO_2 in MOS devices. ZrO_2 thin films have received substantial attention because of the large band gap (ca. 5.5 eV) and the large K in the range of 20-30 [27]. These are expected to become a major candidate for gate dielectric material in LSI technology.

Future Research Directions

The MIS structures have been fabricated and investigated for their electrical characteristics, and the results have been found according to the literature. The electrical characteristics of the devices fabricated have shown how the insulator layer has affected the devices and given the performance of the devices. In the future, to further understand the performance of these devices, which will further help in the technological advancement of the MOS structures, which are the most important and vital in semiconductor devices?

MIS structures fabricated for this project are capacitors, and with the electrical properties obtained, characteristics could be related to actual MIS diodes, which are to be used in semiconductor devices, including varactor diodes, etc. Hence, with the electrical properties obtained, it will assist the possible properties of the semiconductor devices to be fabricated, and possible improvement could be done on the semiconductor devices.

Other than that, with the improvement of technology in semiconductor devices, the devices are in need to be more efficient in terms of power consumption as well as smaller in actual size. Further work can also be done on the miniaturization of the devices fabricated and how to achieve the same electrical properties in much smaller scaled devices. From this, the future generation of these devices can be simulated, and possible characteristics of the devices can be fabricated. This is proven to be very efficient as it can save a tremendous amount of time as well as cost for trial and error of fabricating the actual devices. With the simulation of the future generation devices, the performance can also be predicted. High-K dielectric materials are advancing and will be possible for semiconductor devices. Therefore, the same devices can be fabricated using a higher K dielectric constant insulator layer, and the comparison of the new devices and the old devices can be investigated. Last but not least, studies of the surface states and the improvement of the insulator-semiconductor interface with the use of different methods and the comparison will further enhance the understanding of the behavior in MIS structure devices.

Device Optimization

Summary: Device optimization is a parameter that determines the suitable condition for electrical use and finds the maximum or minimum value for electrical needs. In this project, the analysis focuses on the capacitance and current voltage characteristic of MOSCAP with high-k dielectric, specifically using Al_2O_3 as the dielectric material. The goal is to compare it with another device to determine the material that needs optimization. Two materials, Al_2O_3 and HfO_2, will be used for comparison, both having the same characteristic as the p-n junction in the devices.

The current voltage value is used to determine the ideal factor in device optimization, where a large value indicates a non-optimal condition. The ideal factor and contrast will be compared using the same type of p-n junction MOSCAP device with Al_2O_3 and HfO_2. The comparison of results will be shown in the CV curve and IV.

The CV curve of the p-n junction device shows a characteristic similar to the MISCAP CV curve, with a decrease in C value as V value increases. Since the capacitance of the p-n junction and p-n junction MOSCAP is the same, the CV curve for both devices is also the same. The difference between HfO_2 and Al_2O_3 lies in the gradient of the curve, as Al_2O_3 has a lower k value, resulting in a lower C value compared to HfO_2. However, the ideal factor for each device is significantly different, even though it is close to a value of 1. This is because the C value for the ideal factor is never stable and constantly changes with the changing V value. In contrast, HfO2 achieves a stable C value for the ideal factor with a delay in creating the MISCAP device.

Integration with Other Technologies

Various methods have been used to increase the positive flatband voltage and/or decrease the interface state density of the SiO_2/semiconductor systems. One of the most effective methods has been to grow an ultrathin SiO_2 layer on the silicon and then re-

oxidize in N_2O. In our case, we decided to employ the N_2O anneal directly after the oxide deposition. The C-V curves for the high--K MIS system with the N_2O annealed oxide as well as a similar high-K MIS system that has a thin SiO_2 layer between the high-K oxide and the silicon substrate [28]. The higher k-value of the high-K oxide is quite evident in the comparison. A positive shift in the flatband voltage as well as lower frequency dispersion is observed for the samples with the high-K dielectric. These are strong indications of lower interface state density [29]. The more effective method of the N_2O anneal with the high-K oxide is attributed to the ability of the N_2O to oxidize the Si substrate and the interface between silicon and SiO_2. The very high electro negativity of O_2 and N_2O enables these oxides to remove Si substrate oxide and SiO_2 in order to reform the SiO_2 with an oxygen-rich environment and therefore minimal SiO_2 bond breaking. The effects of the N_2O anneal on the high-K oxide were studied using RBS to depth profile the films [70]. The RBS system uses a He ion beam between 1-2 MeV to scatter off target nuclei. Recoil detection is then used to detect and calculate the energy of the backscattered ions. The known range of ions in a given target allows the depth of the target to be measured. The backscattering cross-section and scattering angle can also be used to measure the concentrations and crystalline properties of the target. High-K and standard thermal oxide samples were annealed in N_2O and analyzed using the RBS.

Implications and Future Directions

This was the first study which was based on the High-k and crystalline Al_2O_3 complex dielectric layer on p-Si which was deposited using solution-based and ALD method. We already mentioned the differences and similarities between different Al_2O_3 dielectric layers at introduction. The MIS structures were fabricated to investigate the electrical characteristics. Analysis of the C-V characteristics showed the presence of a flatband voltage shift, which increased with increasing the thickness of the Al_2O_3 layer. The result showed that the flat band shift/mm is almost constant, so it suggested that the flat band voltage shift is caused by the fixed charge density and it is independent of the $t_{\_Al2O3}$. It is possible to analyze the charges in the Al_2O_3 layer by using the relationship Q = FS, therefore the fixed charge density is found to be approximately 1.9-4.6 C/cm^2. This results in the flat band voltage shift. For a SiO_2 layer, the fixed charge density is sometimes attributed to with Oxygen vacancies in the layer. It is also possible that there are impurities in the Al_2O_3 solution that cause the flat band voltage shift. For device with the $t_{\_Al2O3}$ layer deposited by ALD method, the flat band voltage shift become larger compared with the device using solution based method. It can be considered the cause for this difference is the purity/quality of the Al_2O_3 layer between both of the method. The best result for the fixed charge density is obtained from the $t_{\_Al2O3/\ Al2O3}$ stack structure. This may imply that the interface between Al_2O_3 layer and the next layer is crucial for the determination of the fixed charge in the Al_2O_3 layer.

Conclusion

Tin/Al_2O3/p-Si MIS device has been proven to replace SiO_2 as an insulation material in MOS devices to overcome leakage current, particularly in p-Si. Investigation on the various properties of the MOS devices has been carried out and it has been observed that the devices are very stable. Most of the analysis has been done in 8.5M KOH. The analysis is meant to simulate the behavior of the devices in a wet environment. Varieties of the surface potential and oxide charges evaluations have been done based on the C-V characteristics and mid C-V characteristics. Extremely low charge or discharge trapping, midgap trapping, and oxide charges seen in the C-V plot are an advantage for MIS devices. The devices also provide a very consistent capacitance, which is close to an ideal MIS capacitor. This shows the reliability of the devices. IV characteristics prove that the devices have high current density and field-dependent conduction. This is an advantage for high-k oxide MIS devices. Thus, the aim to have p-Si MIS devices with stable high-K dielectric has been achieved due to the very little trapping and oxide charges. But the requirement of having only a few charges is still a paradox to be solved. As an overview, the devices are very stable with very low charge traps. More investigation must be done on other alternative high-k thin films that show the ability to prevent charges moving in and out of the dielectric by having properties similar to an ideal high-k dielectric. Changes in the properties might increase the stability of the devices, particularly the doping level of the semiconductor, and determine the effect when using very thin oxide films. A proposal that shows the

ability to sustain charges and prevent oxide charges penetration is possible by using a charge blocking layer above the dielectric. This will provide a better future for MIS devices with very low charge liberalization. The research presented in the paper elucidates the pivotal role of high-k dielectrics in Metal-Insulator-Semiconductor (MIS) devices and semiconductor technology at large. Key findings underscore the significance of high-k materials in addressing challenges associated with device miniaturization, including reduced leakage currents, enhanced gate control, and improved scalability. Moreover, the paper highlights the potential solutions and mitigation strategies for limitations such as electron tunneling in thin high-k layers, offering a balanced perspective on high-k MIS devices.

Novel insights from the research include the importance of material engineering and process optimization in tailoring high-k dielectrics to meet the demands of advanced semiconductor devices. Additionally, the exploration of advanced transistor architectures and integration with other materials opens new avenues for enhancing device performance and reliability while mitigating tunneling effects.

Overall, the paper contributes to the field of high-k device technology by providing comprehensive insights into the current state-of-the-art, identifying challenges, and proposing strategies for future advancements. By addressing these issues, the research paves the way for the continued development and integration of high-k dielectrics in semiconductor devices, ultimately driving innovation and progress in electronic technology.

Author Contributions

All authors were involved in conceiving and designing the study. LMI conducted material preparation, data collection, and analysis. The initial draft of the manuscript was authored by LMI, and all authors provided feedback on earlier iterations of the manuscript. All authors have thoroughly examined and given their approval to the final manuscript version.

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Data Availability

The datasets analyzed during the present study can be obtained from the corresponding author upon reasonable request

Declarations

Conflict of Interest

The authors have not provided any information regarding competing interests

Ethical Approval

This study does not involve any human-related data, and no animals were utilized in the research

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